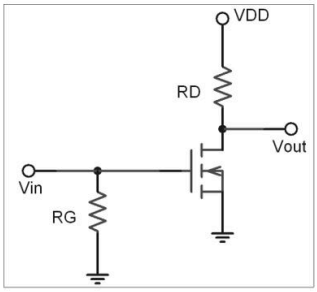
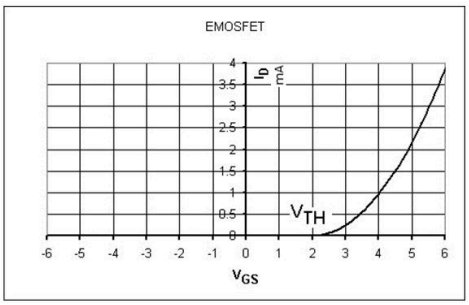
E-MOSFET Switching Circuits

As mentioned before, E-MOSFETs are best used as switching devices. They are typically used in either of two ways: as single transistor switches and as Complementary switching pairs in CMOS logic.

Single Transistor Switch

The component arrangement for a single transistor E-MOSFET switch is pretty similar to the BJT. However, the design must be based upon V_{GS} instead of I_B, as was the case for the BJT. Here's an example that will help us determine what we need to do to make a simple logic switch work.





1. If the minimum guaranteed input voltage is +3.5 V, what Drain current should be used when designing this circuit?

   500 μA

2. If V_{DD} is +5.0 V, determine the minimum value for R_D 10 kΩ, then choose an available 10% resistor value that is close to double your calculated value to ensure the transistor saturates: 18 kΩ

3. When V_{in} is LOW (0 V), what voltage do you expect to see at V_{out}? 5 V

4. When V_{in} is HIGH (>3.5 V), what do you expect to see at V_{out}? 0 V

5. What logic function does this switch perform? NOT (inverter)

6. What would the output voltage be if the input was +2.75 V? 1.4 V. Is this a clear logic level?

   No

Notice that we didn't have to do any calculations for R_G. That's because there is no Gate current, so the value of this resistor doesn't have any bearing on the basic design of the circuit. However, we usually put one, and sometimes two, Gate resistors into our design.

Pull-up or Pull-down Resistor

The resistor shown above is a pull-down resistor. If, for some reason, V_{in} was not connected, with no other components at the Gate any small residual charge or accumulated charge from static electricity would generate an unexpected and unpredictable V_{GS}, which could turn on the transistor. We didn't need to worry about that with our BJT switches, because their natural condition was OFF, and with no source of current connected, there was no chance of the BJT turning on.

The pull-up or pull-down resistor provides a path to either a positive voltage source or ground that will dissipate any charge on the Gate and provide a known input voltage. Using a resistor allows us to connect the signal source and over-ride the pull-up or pull-down resistor.

7. In the circuit above, the pull-down resistor establishes an input LOW if the signal source isn't connected.

Capacitive Surge Current Resistor

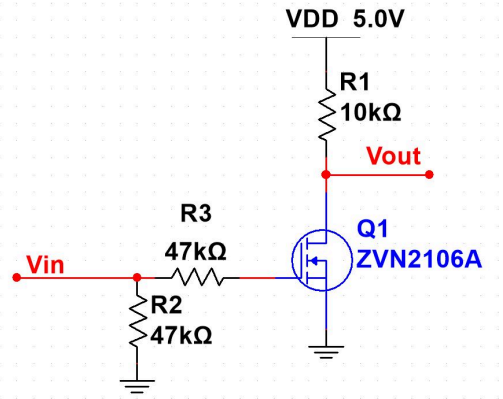
The other resistor that is frequently used at the Gate is put in ***series*** with the input voltage and the Gate. As you know, the voltage of a capacitor cannot be instantaneously changed, and the faster the rate of change of voltage the higher the current required to charge the capacitor. The surge current-limiting resistor provides the exponential charge characteristic you learned about in a previous course which slows down the response but protects the equipment.

For small FETs like the ones we use, this surge current is pretty minimal, and the resistance in the wires or PCB traces can be enough to limit the surge current. However, for bit power FETs, the capacitance can be pretty big, even to the point of necessitating BJT drive transistors to turn them on fast enough for applications like power inverters.

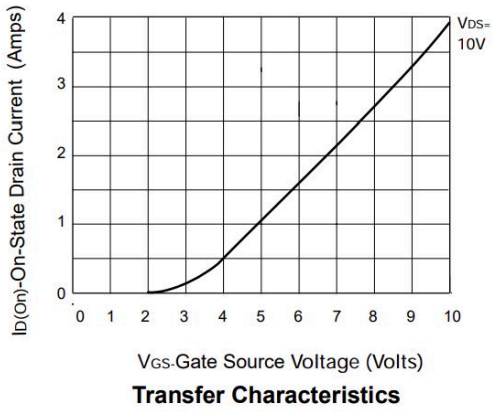
If you install both a surge current resistor and a pull-up or pull-down resistor, put the surge current resistor on the Gate side of the pull-up or pull-down resistor.

N-Channel E-MOSFET Logic Switch

Here's a worked example using an N-Channel E-MOSFET that's pretty close to the ones in your component kit. In this case, it's operating as a simple inverter.



The input for this circuit is 3.3 V TTL logic, switching between 0.0 V and 3.3 V. The first question we need to ask is whether this transistor will switch appropriately. Here's a tranfer curve from the data sheet:



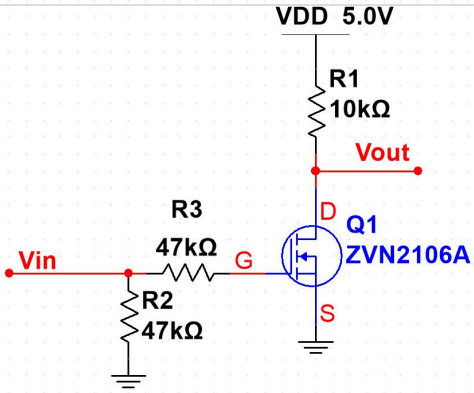
Transfer Characteristics

The first thing to notice is that I_D is in amps! This little transistor can handle a lot of current!

More to the point, if V_{GS} is 3.3 V, the transistor can pass about 400 mA, so there's no problem with us using it in our circuit. Proof?

I_{Dmax} = 5 V / 10 kΩ =500 μA, which is about a thousandth of the current that could be provided by the transistor.

We should always label the pins so we don't get confused. Here's the labelled diagram:



When V_{in} is 0.0 V (LOW), V_G = 0 V and V_S = 0 V (grounded), so V_{GS} = 0 V and I_D will be 0 mA. With no voltage drop across R_D, the output will be at +5.0 V (HIGH). The transistor behaves as an open switch.

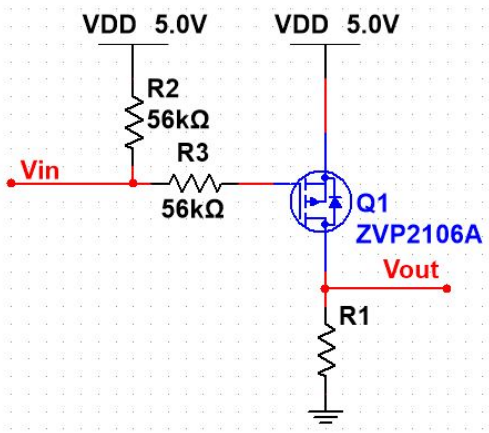
When V_{in} is 3.3 V (HIGH), V_{GS} = 3.3 V which is past the threshold shown on the graph and also past the highest (worst) value for V_{TH} given in the Data Sheet (https://www.diodes.com/assets/Datasheets/ZVN2106A.pdf) as 2.4 V, so the transistor will be turned on. From our previous discussion, it will be saturated, so its on resistance, given in the data sheet as 2 Ω, will result in V_{DS} = 500 μA * 2 Ω = 1 mV, or practically zero (LOW). The transistor behaves as a short or a closed switch.

If V_{in} is accidentally left disconnected, R2 will dissipate to ground any charge that might collect on the Gate, pulling the Gate to 0.0 V and turning the transistor off (output will be HIGH).

When V_{in} switches from LOW to HIGH, the Gate capacitance will charge through R3, and when V_{in} switches from HIGH to LOW, the Gate capacitance will discharge through R3.

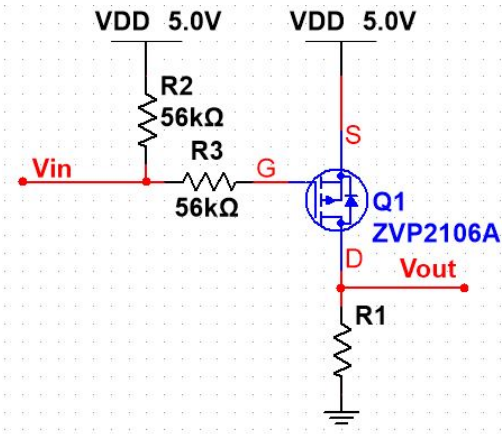
P-Channel E-MOSFET Logic Switch

Now, let's do a P-Channel E-MOSFET switch.



Notice that the symbol for this transistor contains a protection diode, reverse-biased across the device. The same protection would be found in the ZVN device in the previous question, but the library designers left it out.

Before we get too far, we'd better label the pins. Note that the Source is "up" and the Drain is "down", as would be expected for a P-Channel device.



We'll design this switch to be low-power: only about 250 μA in the ON condition. Since the voltage drop across the transistor V_{DS} will be very small (the Data Sheet (https://www.diodes.com/assets/Datasheets/ZVP2106A.pdf) indicates an ON resistance of 5 Ω, so V_{DS} = -1.25 mV (negative because D is below S)), we can treat the transistor as a short or closed switch. In other words, essentially the full 5 V will appear across R1, so R1 = 5 V / 250 μA = 20 kΩ. Since we only have 10% standard values, we'll pick 22 kΩ (larger to force saturation).

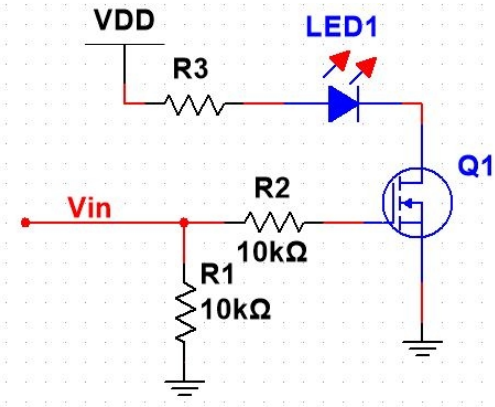
We'll check to see if the transistor will really saturate. The data sheet says that the worst value for V_{TH} is -3.5 V. So, if Vin is zero, $V_{GS} = V_G - V_S = 0 - 5.0$ V = -5.0 V. That's considerably bigger than V_{TH}, so the transistor should be ON. From the graph of the transfer function, at -5.0 V I_D could be as big as approximately -400 mA, so the transistor will definitely be able to supply the 250 μA we are designing for. Actually, the theoretical current for the resistor we chose will be 5 V / 22 kΩ = 227 μA.

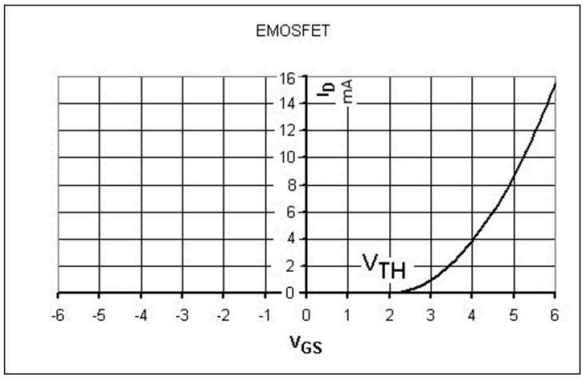
As with the PNP BJT switch, the problem with this circuit will be turning it off, as we will have to raise the Gate voltage high enough to ensure we're above the threshold. The data sheet indicates that it's possible for a transistor to be as good as having V_{TH} = -1.5 V, so to turn the transistor off, we need an input voltage of greater than 5 V - 1.5 V = 3.5 V (from $V_G = V_S + V_{GS}$). So, this circuit would not work reliably with a 3.3 V logic input. It would be fine, however, with 5 V TTL logic.

If the input was accidentally left disconnected, R2 would pull the Gate HIGH, resulting in V_G = 5.0 V. In this case, $V_{GS} = V_G - V_S$ = 5 V - 5 V = 0 V, so the transistor will be off. With no current through R_D, the output would be at 0.0 V, or LOW.

E-MOSFET Current Switch

As with the BJT, we can use the FET as a switch to turn a current on or off to control LEDs, lights, relays, heater elements, motors, etc. Here's a simple LED driver using a transistor with significantly less current handling capacity than the ones in your kits, with both of the Gate resistors installed.





8. If the LED has a barrier potential of 1.7 V and requires at least 6 mA to glow visibly, will this circuit work with an input that switches between 0 and +5 V? Yes

9. The available power supply is +9 VDC. Calculate the ideal resistance for R3. 1.22 kΩ, then pick the next lowest 10% resistance value 1.2 kΩ.

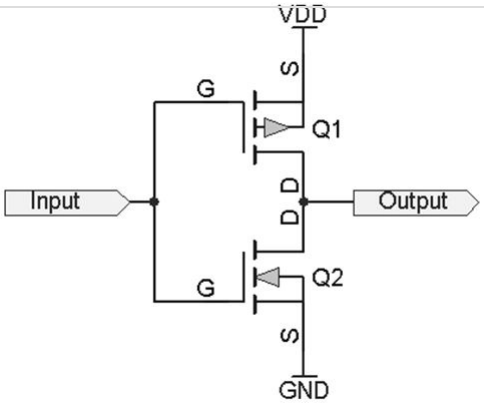
10. When should the LED glow? When the input is …

11. If, by mistake, the series gate resistor had been placed ahead of the pull-down resistor, what voltage would appear at the Gate when the input is HIGH? 2.5 V Would this provide sufficient current to turn the LED on fully? No

CMOS Switch

We've finally made it to the switching circuit that has revolutionized digital electronics, and has made the E-MOSFET the most common resistor by far -- probably over 99% of earth's transistors are found in CMOS switches, because that's what is used in all of our computers, portable phones, and so on.

Here's the basic CMOS switch, which is the E-MOSFET version of the Totem Pole configuration:



Two transistors, no resistors -- pretty simple! Note that the upper transistor is P-Channel and the lower transistor is N-Channel. These form a complementary pair of E-MOSFETs, hence the name: Complementary Metal Oxide Semiconductor.

There is no need for biasing resistors in this design, because, in either of its static states, one transistor is turned off, so no current flows, and no power is dissipated.

12. When the input is LOW, Q1 is [ON] and Q2 is [OFF] In this state, the output is directly connected to [VDD] and the output is [HIGH]. The current from VDD to GND is [0]
13. When the input is HIGH, Q1 is [OFF] and Q2 is [ON] In this state, the output is directly connected to [GND] and the output is [LOW]. The current from VDD to GND is [0]
14. Based upon what you have discovered, this device is a logical [NOT (inverter)]
15. How much power is dissipated when the input is LOW? [0] mW
16. How much power is dissipated when the input is HIGH? [0] mW

From what you've just done, you've shown that the CMOS switch can provide both logic HIGH and logic LOW without any current, and therefore with no power dissipated as heat, as P=IV. This is the reason CMOS can be used in extremely computationally powerful devices like computers and phones. However, these devices still produce some heat, and your computer probably has a fan and maybe even liquid cooling, if you're a serious gamer. Where does that heat dissipation come from?

When a CMOS switch makes the transition between one logic level and the other, there is a split-second of time when both transistors are turned on. During this time, since there are no current-limiting resistors in the circuit, the transistors are effectively trying to short the power supply to ground, and a great deal of current can flow. The accumulated effect of millions of these transitions per second can lead to a significant amount of heat being produced.

The solutions to the heating problem are typically

- Speed up the transition time so the current burst is as short as possible
- Lower the voltage of the power supply, because P=IV, so a lower voltage means less power
- Reduce the overlap between the threshold voltages of the two transistors so that the percentage of time they are both on is reduced

Of course, in our relentless pursuit of technological advancement, as soon as we reduce the power dissipation, we speed up our devices! So, power dissipation will always be an issue.

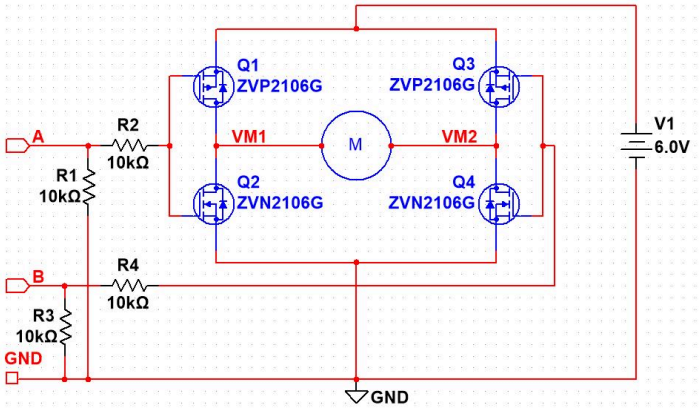
CMOS Issues

1. We've seen that the overlap of threshold voltages in CMOS switches results in heat dissipation.
2. Another problem caused by this overlap is that CMOS inputs must always be held at a defined logic level. If a CMOS input is allowed to float, it will -- any static electrical charge available will collect on the Gates, and will very likely result in an input voltage between LOW and HIGH, where both transistors will be turned on. With no current-limiting resistors, something is going to experience Thermal Destruction, and the device will be destroyed. The solution is to ensure that all CMOS ***inputs*** (don't mess with the outputs) must be pulled or tied HIGH or LOW. Many modern devices have weak internal pull-up or pull-down resistors to protect them, but these resistors add to the overall power dissipation of the device.
3. A third problem caused by the threshold voltage overlap is that each logic transition puts a voltage spike onto the power supplies, as the voltage is pulled down towards ground and then recovers. This can interfere with the operation of other ICs in the device, and can generate electromagnetic radiation (EMR) that could interfere with other sensitive devices such as radio-based equipment or heart pacemakers. The solution to this problem is the careful use of ***decoupling capacitors***. Each CMOS device power pin should have a capacitor to ground as close to the device as possible. Since the voltage across a capacitor cannot be changed instantaneously, the CMOS switching spike will not be able to pull the power supply to ground. In other words, the decoupling capacitor will provide the instantaneous charge demands of the CMOS switch as it changes logic levels.
4. Electrostatic Discharge damage -- the thin oxide layer at the Gate is quite easily damaged. A "spark" of 30 V or more is likely to cause irreparable damage. Dropping a piece of paper onto a CMOS chip is likely to generate more than 30 V, and a visible or tangible "shock" is likely to be in the hundreds or thousands of volts -- definitely enough to kill a CMOS device. Many devices have ESD protection built into them, but CMOS devices should only be handled when the handler is wearing an electrostatic dissipative (static) strap that is properly grounded or held at the potential of the device being worked upon.
5. A completely unrelated problem that arises with CMOS devices is called ***latch-up***. This is a problem that arises from having hundreds of CMOS switches made on the same layers of semiconductor material. in places other than where the desired circuitry has been built, there will be material that forms unexpected semiconductor devices that are outside of the control of the circuit. These vestigial devices can sometimes go into reverse breakdown, attempting to short power to ground, and there is no way to turn them off other than to shut off the power to the IC. Latch-up only happens if a CMOS input is pulled to a voltage either above the power supply voltage or below ground. Some devices have clamping circuits built into their inputs, but it is wise never to allow out-of-range input voltages to reach a CMOS device.

As long as these limitations and issues are properly addressed in the design of a piece of equipment, CMOS can provide long and trouble-free service with very low power consumption.

CMOS H-Bridge

It should probably have crossed your mind that the CMOS switch is essentially a FET Totem-Pole or Half-Bridge, so it's just a small step to creating a CMOS H-Bridge. The following is a worked example to help you firm up your understanding of the CMOS switch and also show you the operation of a CMOS DC motor controller.



First, a quick investigation. The inputs are coming from off-board, likely from a microcontroller. As always, there needs to be a common ground between off-board equipment and our circuit. Also, note that the two inputs have pull-down resistors, so the default condition is 00. From what we know of H-Bridges, this should be one of the two OFF conditions for the motor. Also, there are capacitive charge-limiting capacitors shared by the Gates of the MOSFETs. Unlike the BJT version, we don't need separate resistors for each transistor, since there's no operating current at the Gate of a FET. Only the voltage matters.

A quick check shows that the Sources of the P-Channel devices are connected to the positive power rail and the Sources of the N-Channel devices are connected to ground, which is as it should be.

All of the MOSFETs have internal protection diodes, so we don't need to install our own. Also notice that, with the transistors installed correctly, all the internal diodes are reverse biased, as they should be.

Another important thing to notice is that the motor-side of this circuit is powered by its own 6 VDC circuit. We can probably assume that the logic levels are 0.0 V and 5.0 V, so we'll have to make sure the input voltage goes high enough to shut off the P-Channel devices. Let's do that. The Data Sheet (https://www.diodes.com/assets/Datasheets/ZVP2106A.pdf) for the ZVP2106G indicates that the smallest value for V_{TH} is -1.5 V. So, with a 6 VDC power rail, we need to have the input logic rise above 6 V - 1.5 V =4.5 V, so as long as our input signal HIGH is 5.0 V, this circuit will work. *(If it hadn't, we'd have needed to provide Level Translators to bring the HIGH voltage up to 6 V.)*

Now for a quick analysis:

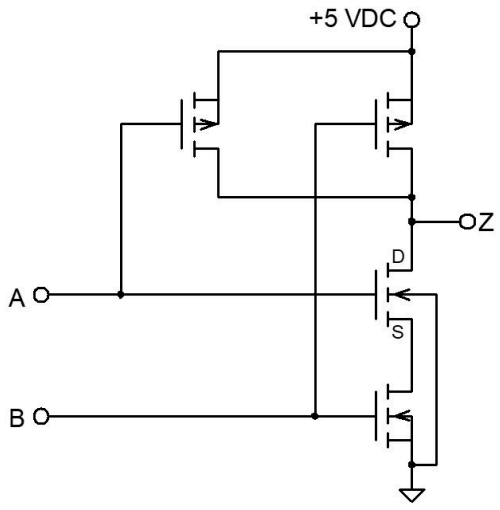
- When an input is LOW
  - V_{GS} for the P-Channel device will be V_G - V_S = 0 V - 6 V = -6 V, which is much greater than the worst V_{TH} of -3.5 V, so the transistor will be ON, connecting the Drain and therefore the motor connection to +6 V.
  - V_{GS} for the N-Channel device will be 0 V - 0 V = 0 V, so the transistor will be OFF, disconnecting the Drain and therefore the motor connection from ground.
- When an input is HIGH (+5 V)
  - V_{GS} for the P-Channel device will be V_G - V_S = 5 V - 6 V = -1 V, which is less than the smallest expected V_{TH}, so the transistor will be OFF, disconnecting the motor connection from the positive rail.
  - V_{GS} for the N-Channel device will be V_G - V_S = 5 V - 0 V = +5 V, which is higher than the largest expected V_{TH} of 2.4 V, so the transistor will be ON, connecting the motor connection to ground.
- So, when both inputs are LOW (00), both motor connections will be at 6 V, no current will flow, and the motor will be OFF.
- When A is LOW and B is HIGH (01), Vout1 will be 6.0 V and Vout2 will be 0.0 V, so current will flow through the motor from left to right (assume "forward").
- When A is HIGH and B is LOW (10), Vout1 will be 0.0 V and Vout2 will be 6.0 V, so current will flow through the motor from right to left (assume "reverse").
- When both inputs are HIGH (11), both motor connections will be at 0.0 V, so current will flow, and the motor will be OFF.

The (11) input logic condition is the safest way to turn the motor off, because all the lines will be de-energized and accidental shorting won't damage anything.

CMOS Logic Gates

Various combinations of complementary E-MOSFET transistors are possible, giving rise to all of the logic gates you encounter in courses like your Digital Logic course. Here are two examples for you to analyze. For each transistor, determine V_{GS} to help you tell if the transistor is ON or OFF (V_{GS} = 0 means OFF for an E-MOSFET). From that, determine whether the output, Z, is connected to +5 VDC or Ground. Fill in the table and use it to determine which logic gate this is.

17. Circuit #1

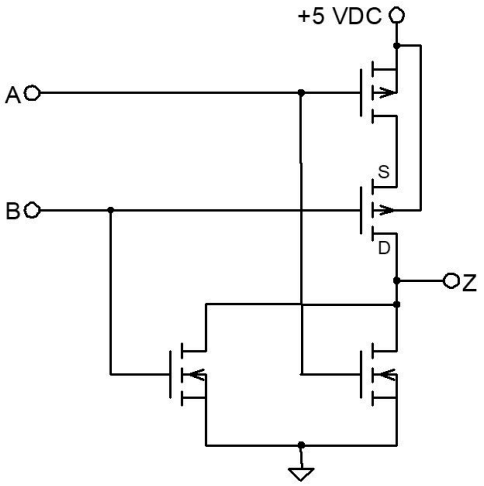


A	B	Z
0 V	0 V	5 V

0 V	+5 V	5 V
+5 V	0 V	5 V
+5 V	+5 V	0 V

This logic gate is NAND

18. Circuit #2



A	B	Z
0 V	0 V	5 V
0 V	+5 V	0 V
+5 V	0 V	0 V
+5 V	+5 V	0 V

This logic gate is NOR